ECEN 429011.201820: Introduction to Digital Systems Design Laboratory

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Lab #1

**Introduction**

For lab 1 our task was to first familiarize ourselves with Xilinx Design and the Digilent Basys 3 FPGA Board that we are going to be coding on. During these steps we learned how to configure the settings on Xilinx for our board and how to load a program to the board. We also have three programming assignments for this lab. The first assignment was to write a simple VHDL code using an AND gate with two inputs and one output. The second assignment was to write a VHDL code using the car alarm example which was also used in class. Car alarm insist of 3 inputs using switches and 2 outputs using LED lights. The third assignment was to create our own design implementation and write a VHDL code using only 4 inputs and 3 outputs.

**Background, Design Solution and Results**

Program 1 uses A and B as inputs for an AND gate and C as an output

|  |  |  |  |
| --- | --- | --- | --- |
| inputs | In inputs(switches & I/O pin #s) | outputs | outputs(LED & I/O pin #s) |
| A A | G SWITCH 1 (V16) | C C | LED 3(V19) |
| B B | SWITCH 7(W13) | D |  |

Truth Table AND gate

|  |  |
| --- | --- |
| AB | C |
| 00 | 0 |
| 01 | 0 |
| 10 | 0 |
| 11 | 1 |

Program 2 part 1 uses A and B for an AND gate and D as an output. Also uses B and C for an OR gate and E as an output.

|  |  |  |  |
| --- | --- | --- | --- |
| inputs | In inputs (switches & I/O pin #s) | outputs | outputs(LED & I/O pin #s) |
| A A | G SWITCH 0 (V17) | C D | LED 7 (V19) |
| B B | SWITCH 1 (V16) | DE E | LED 6 (U14) |
| C | SWITCH 2 (W16) |  |  |

Program 2 part 2 Car Alarm uses D OR V for the OR gate and the OR gate is connected with M to form an And gate to get the output S.

|  |  |  |  |
| --- | --- | --- | --- |
| inputs | In inputs(button,switches & I/O pin #s) | outputs | outputs(LED & I/O pin #s) |
| A D | G BTN L ( W19) | CSS S | LED 0 (U16) |
| B V | SWITCH 15 (R2) | D |  |
| M | BTN R (T17) |  |  |

Truth Table for Car Alarm

|  |  |
| --- | --- |
| DVM | S |
| 000 | 0 |
| 001 | 0 |
| 010 | 0 |
| 011 | 1 |
| 100 | 0 |
| 101 | 1 |
| 110 | 0 |
| 111 | 1 |

**Conclusion**

In this lab we learned how to use Xilinx and the Digilent Basys 3 FPGA Board to implement each assignment in VHDL code. We learned how to map inputs and outputs to different components on the board and also how to run and load programs on the board.